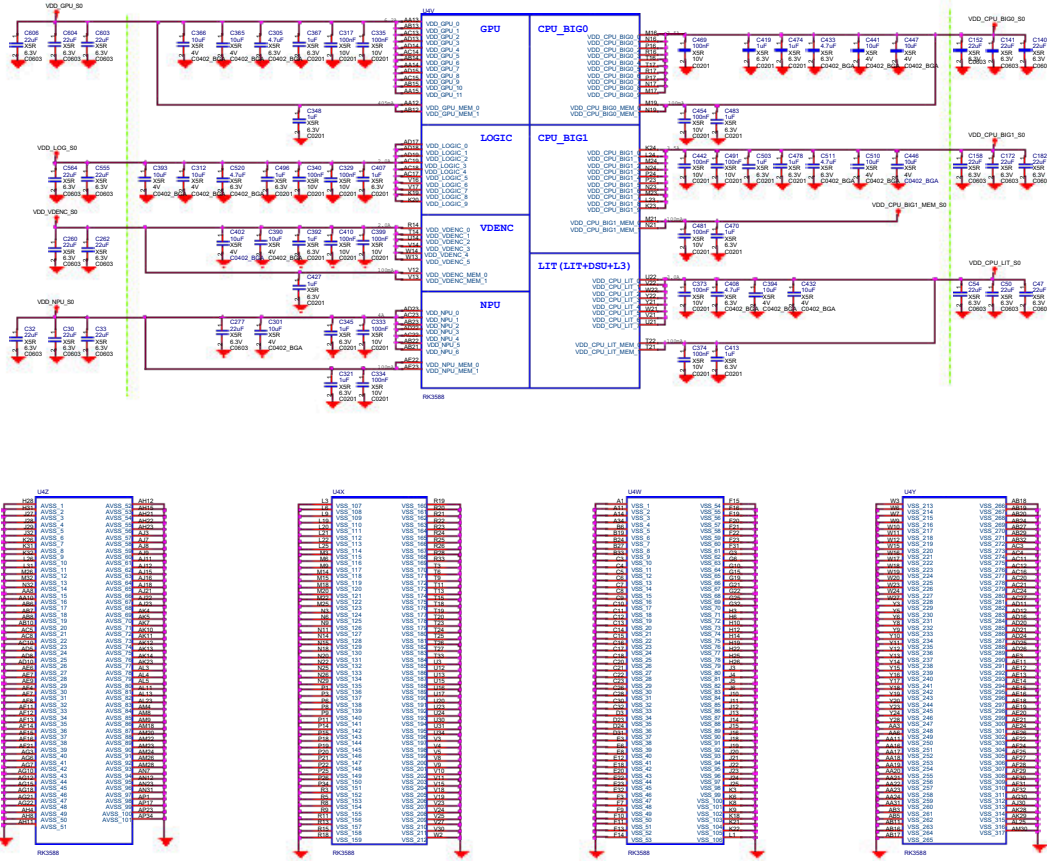


RK3588_V (POWER)



AVSS	AVSS	AVSS	AVSS
AVSS_1	AVSS_2	AVSS_3	AVSS_4
AVSS_5	AVSS_6	AVSS_7	AVSS_8
AVSS_9	AVSS_10	AVSS_11	AVSS_12
AVSS_13	AVSS_14	AVSS_15	AVSS_16
AVSS_17	AVSS_18	AVSS_19	AVSS_20
AVSS_21	AVSS_22	AVSS_23	AVSS_24
AVSS_25	AVSS_26	AVSS_27	AVSS_28
AVSS_29	AVSS_30	AVSS_31	AVSS_32
AVSS_33	AVSS_34	AVSS_35	AVSS_36
AVSS_37	AVSS_38	AVSS_39	AVSS_40
AVSS_41	AVSS_42	AVSS_43	AVSS_44
AVSS_45	AVSS_46	AVSS_47	AVSS_48
AVSS_49	AVSS_50	AVSS_51	

AVSS	AVSS	AVSS	AVSS
AVSS_1	AVSS_2	AVSS_3	AVSS_4
AVSS_5	AVSS_6	AVSS_7	AVSS_8
AVSS_9	AVSS_10	AVSS_11	AVSS_12
AVSS_13	AVSS_14	AVSS_15	AVSS_16
AVSS_17	AVSS_18	AVSS_19	AVSS_20
AVSS_21	AVSS_22	AVSS_23	AVSS_24
AVSS_25	AVSS_26	AVSS_27	AVSS_28
AVSS_29	AVSS_30	AVSS_31	AVSS_32
AVSS_33	AVSS_34	AVSS_35	AVSS_36
AVSS_37	AVSS_38	AVSS_39	AVSS_40
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AVSS_45	AVSS_46	AVSS_47	AVSS_48
AVSS_49	AVSS_50	AVSS_51	

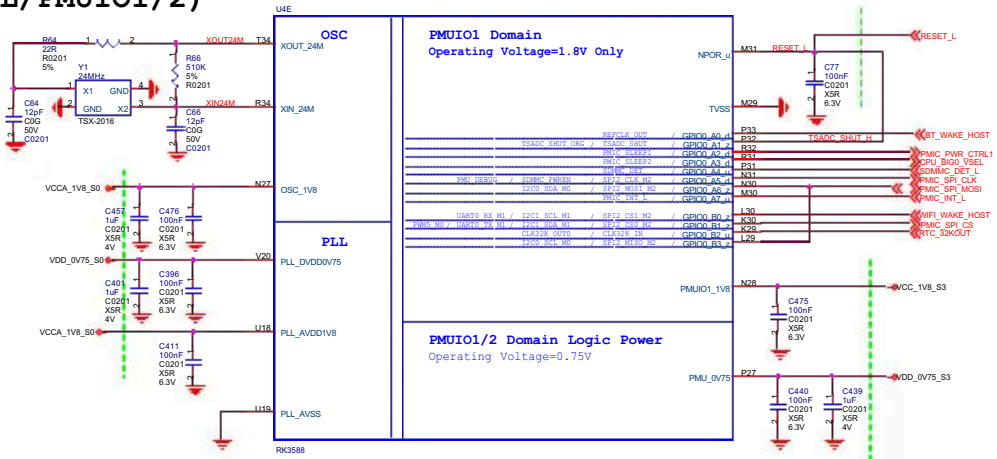
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AVSS_5	AVSS_6	AVSS_7	AVSS_8
AVSS_9	AVSS_10	AVSS_11	AVSS_12
AVSS_13	AVSS_14	AVSS_15	AVSS_16
AVSS_17	AVSS_18	AVSS_19	AVSS_20
AVSS_21	AVSS_22	AVSS_23	AVSS_24
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AVSS_29	AVSS_30	AVSS_31	AVSS_32
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AVSS_37	AVSS_38	AVSS_39	AVSS_40
AVSS_41	AVSS_42	AVSS_43	AVSS_44
AVSS_45	AVSS_46	AVSS_47	AVSS_48
AVSS_49	AVSS_50	AVSS_51	

AVSS	AVSS	AVSS	AVSS
AVSS_1	AVSS_2	AVSS_3	AVSS_4
AVSS_5	AVSS_6	AVSS_7	AVSS_8
AVSS_9	AVSS_10	AVSS_11	AVSS_12
AVSS_13	AVSS_14	AVSS_15	AVSS_16
AVSS_17	AVSS_18	AVSS_19	AVSS_20
AVSS_21	AVSS_22	AVSS_23	AVSS_24
AVSS_25	AVSS_26	AVSS_27	AVSS_28
AVSS_29	AVSS_30	AVSS_31	AVSS_32
AVSS_33	AVSS_34	AVSS_35	AVSS_36
AVSS_37	AVSS_38	AVSS_39	AVSS_40
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AVSS_49	AVSS_50	AVSS_51	

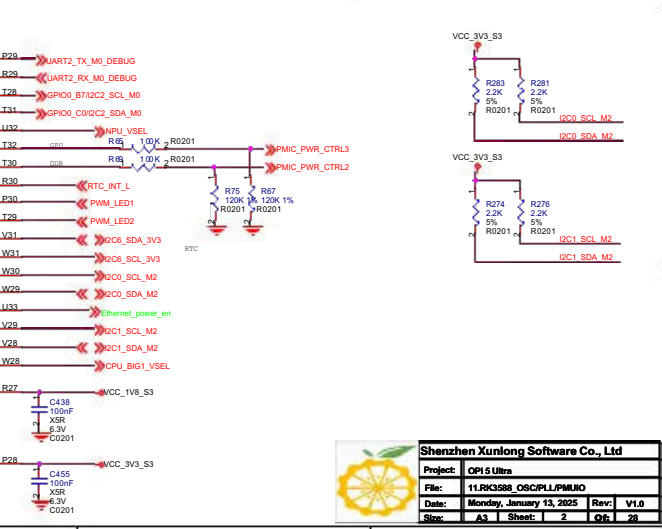


Shenzhen Xinlong Software Co., Ltd
Project: ops 4 Ultra
Date: 2023-09-28
File: RK3588_V (POWER).docx
Page: 1 / 1

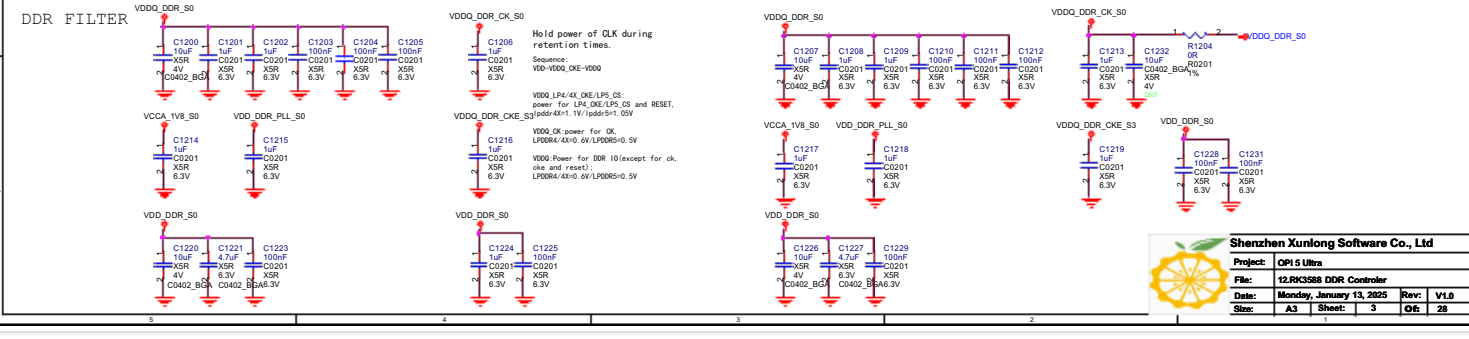
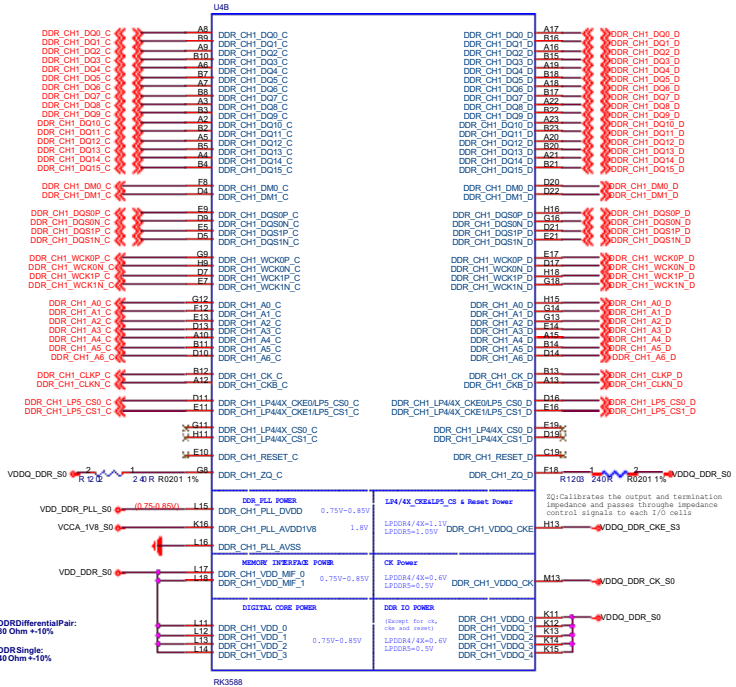
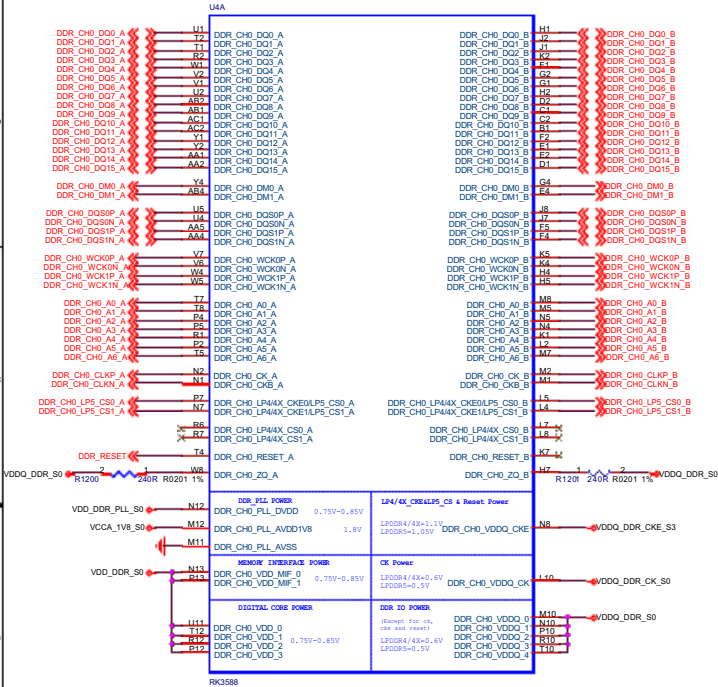
RK3588_E (OSC/PLL/PMUIO1/2)



PMUIO2 Domain		Operating Voltage=1.8V/3.3V	
/ UART2_TX_M0	/	/ I2S1_MCLK_M0	/ PTE13021_1_CLKREQ_M0
/ UART2_RX_M0	/	/ I2S1_SCLK_M0	/ PTE13021_1_WAKEN_M0
/ CAN0_TX_M0	/	/ I2S1_LMCK_M0	/ PTE13021_1_PBSYN_M0
/ CAN0_RX_M0	/	/ ROM0_CLK0_M0	/ PTE13021_0_CLKREQ_M0
/ UART0_RX_M0	/	/ CPU0_CLK0_M0	/ PTE13021_0_WAKEN_M0
/ UART0_TX_M0	/	/ I2S1_S2IO_M0	/ PTE13021_0_PBSYN_M0
/ UART0_RX_M0	/	/ I2S1_S2IO_M0	/ PTE13021_0_WAKEN_M0
/ UART1_RX_M0	/	/ ROM0_S2IO_M0	/ PTE13021_0_PBSYN_M0
/ UART1_TX_M0	/	/ ROM0_S2IO_M0	/ PTE13021_0_WAKEN_M0
/ UART1_RX_M0	/	/ ROM0_S2IO_M0	/ PTE13021_0_PBSYN_M0
/ UART1_TX_M0	/	/ ROM0_S2IO_M0	/ PTE13021_0_WAKEN_M0
/ ROM1_TX0_CEC_M0	/	/ UART0_CTSN	/ ROM1_RX_SDA_M0
/ ROM1_TX1_CEC_M0	/	/ UART0_CTSN	/ ROM1_RX_SDA_M0
/ ROM1_TX0_SCL_M0	/	/ UART0_CTSN	/ ROM1_RX_SDA_M0
/ ROM1_TX1_SCL_M0	/	/ UART0_CTSN	/ ROM1_RX_SDA_M0
/ ROM0_S2IO_M0	/	/ ROM0_S2IO_M0	/ ROM0_S2IO_M0



Shenzhen Xunlong Software Co., Ltd	
Project:	QPI 5 Ultra
File:	11RK3588_OSC/PLL/PMUIO
Date:	Monday, January 13, 2025
Rev:	V1.0
Star:	A3 Sheet: 2 Of: 28



Shenzhen Xunlong Software Co., Ltd

Project: **OP1 6 Ultra**

File: **12_RK3588_DDR_Controller**

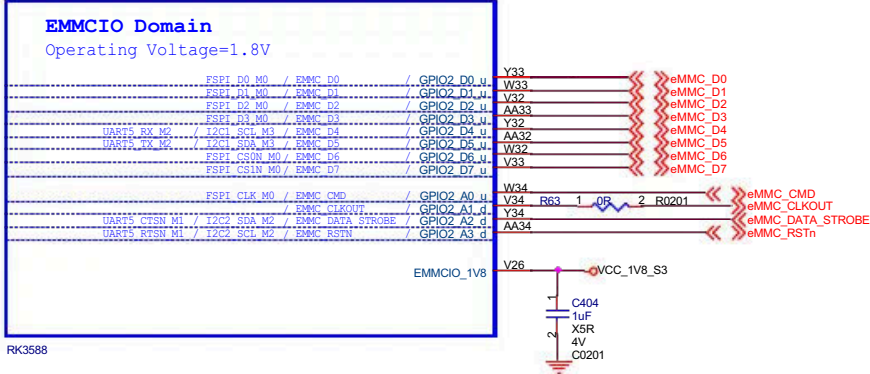
Date: **Monday, January 13, 2025**

Rev: **V1.0**

Size: **A3** Sheet: **3** Of: **23**

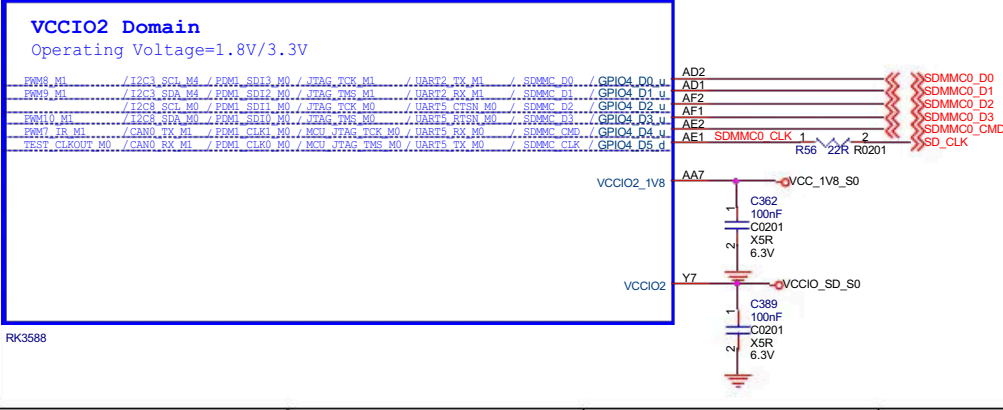
RK3588_C (EMMCIO Domain)

U4C



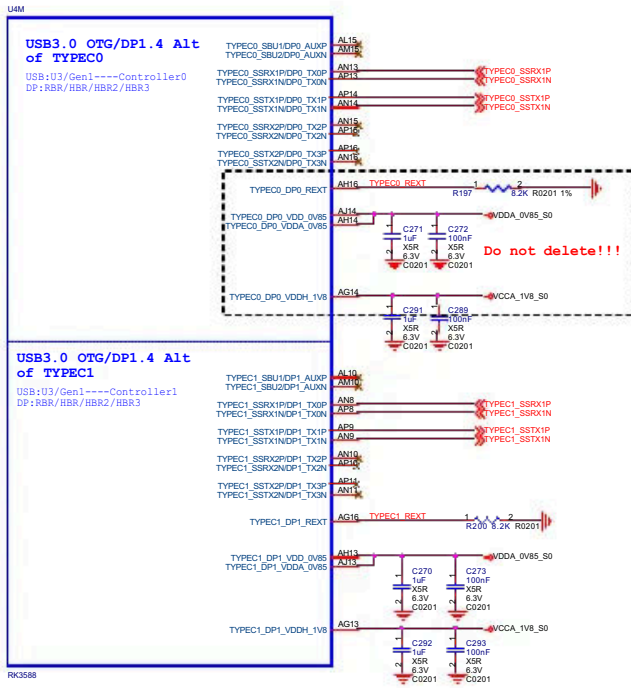
RK3588_D (VCCIO2 Domain)

U4D



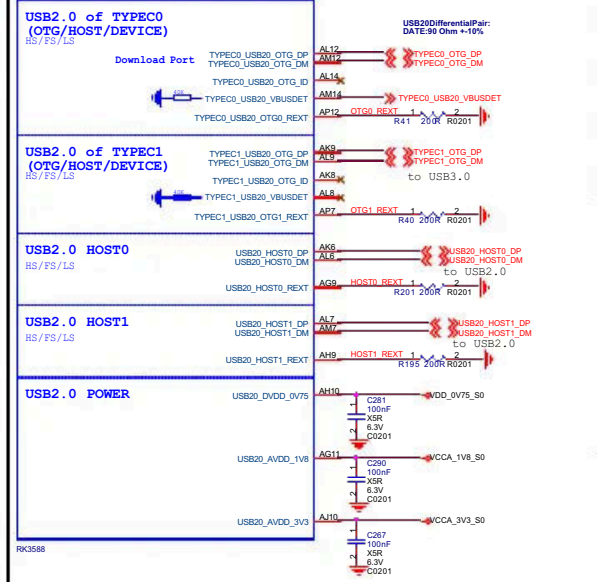
Shenzhen Xunlong Software Co., Ltd			
Project:	OPI 5 Ultra		
File:	13.RK3588_Flash/SD Controller		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	4 Of: 28

RK3588_M (TYPEC/DP)



RK3588

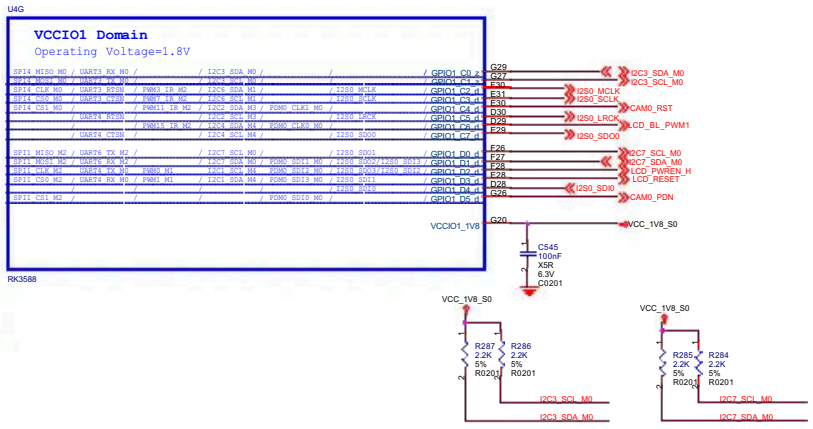
RK3588_L (USB2.0 HOST/OTG)



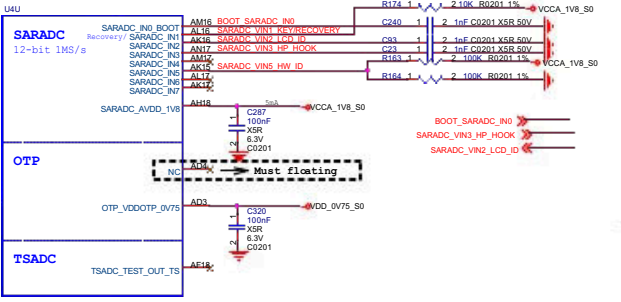
RK3588

Shenzhen Xunlong Software Co., Ltd			
Project:	OPI 5 Ultra		
File:	14RK3588_USB30/USB20_Cst		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	5 of 28

RK3588_G (VCCIO1 Domain)



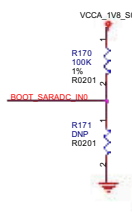
RK3588_U (SARADC/OTP)



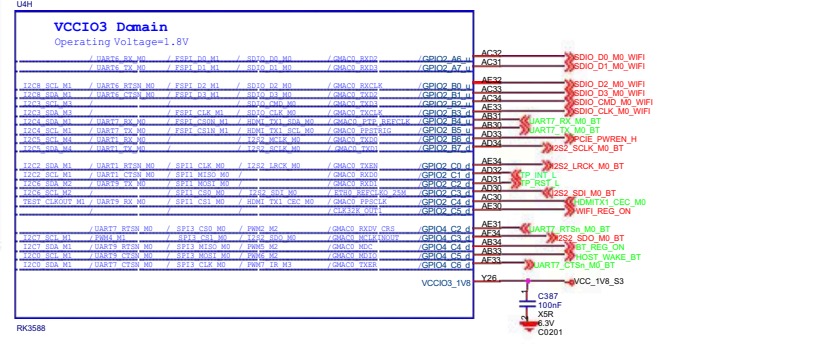
BOOT MODE CONFIG

TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0-EMMC-SD Card-USB



RK3588_H (VCCIO3 Domain)



Shenzhen Xunlong Software Co., Ltd

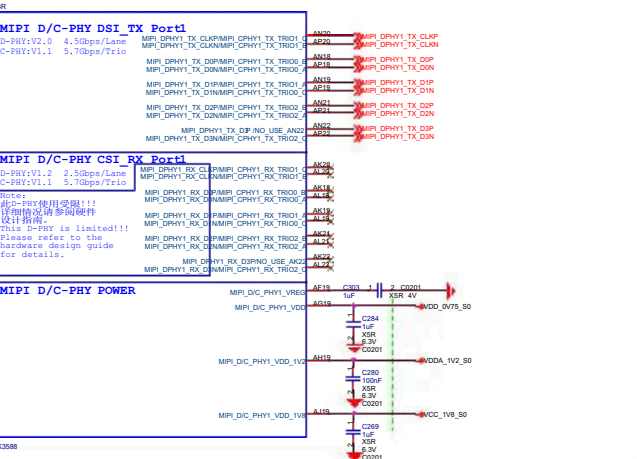
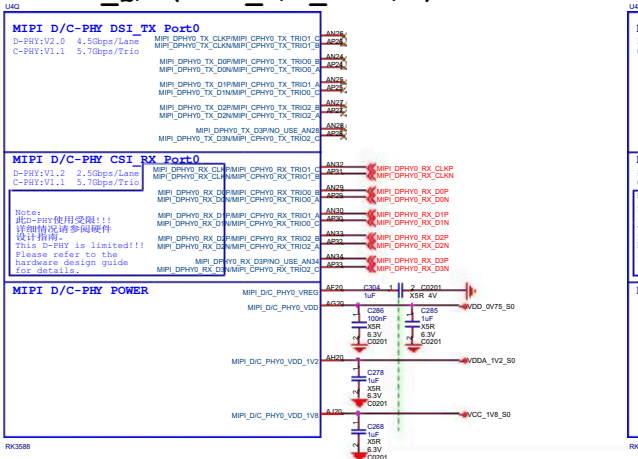
Project: OPI 6 Ultra

File: 15RK3588_SARADC1.8V Only GPIO

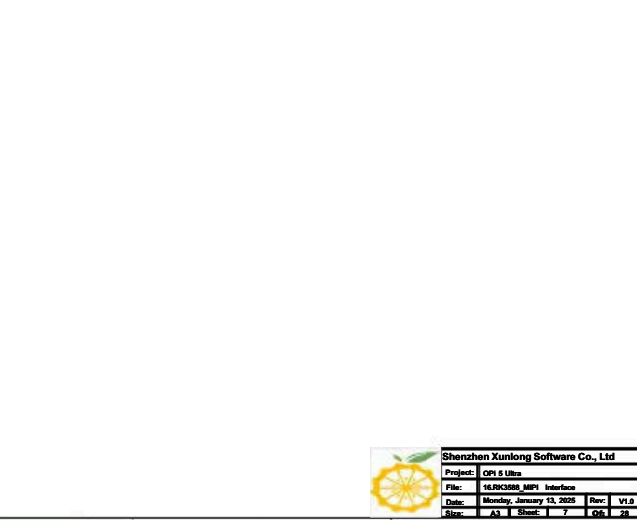
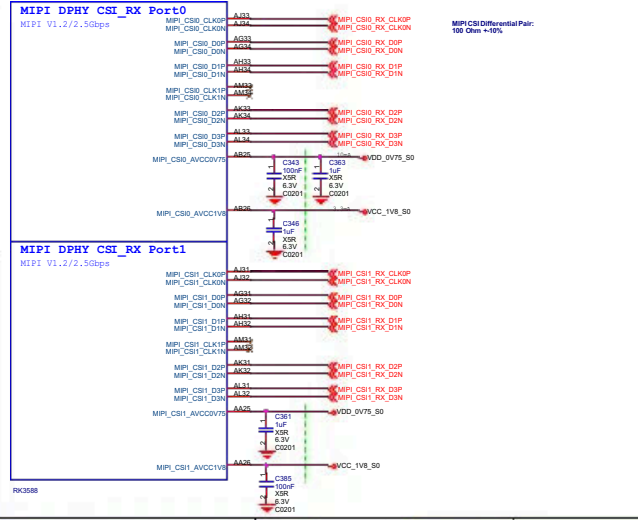

Date: Monday, January 13, 2025 Rev: V1.0

Size: A3 Sheet: 6 Of: 28

RK3588_Q/R (MIPI_D/PHY)



RK3588_P (MIPI_DPHY_CSI_RX_PHY)

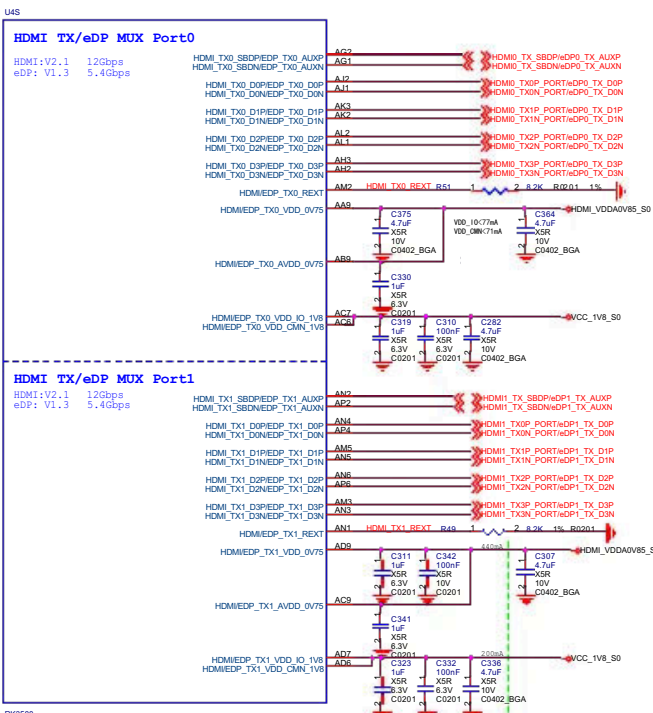



Shenzhen Xuntong Software Co., Ltd

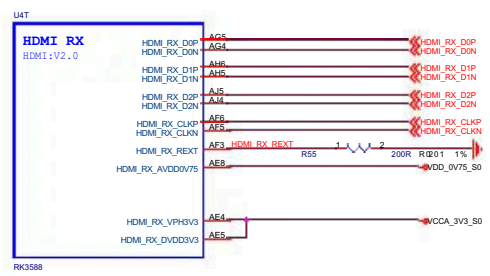
Project:	CSI & USB
File:	647K3588_MIPI_Interface
Date:	Monday, January 13, 2025
Rev:	V1.0
Size:	A3 Sheet 7 of 28

RK3588_S (HDMI2.1 TX)

RK3588_T (HDMI20 RX)

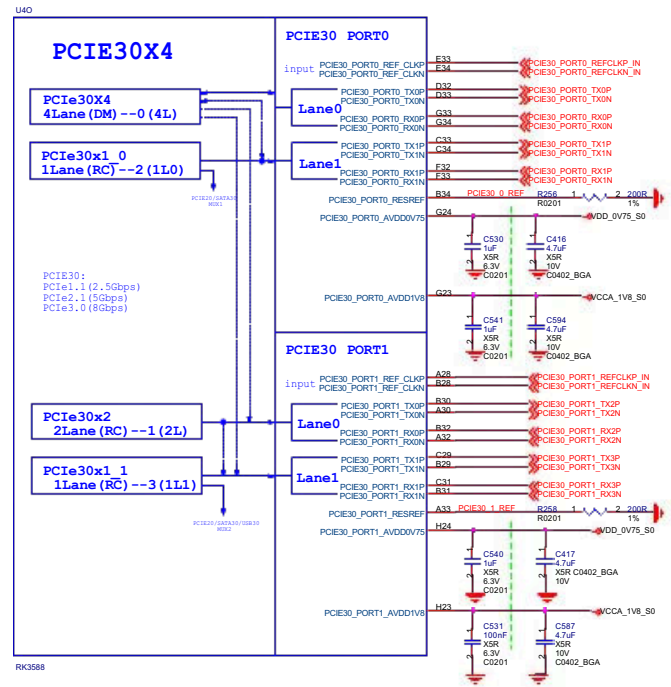
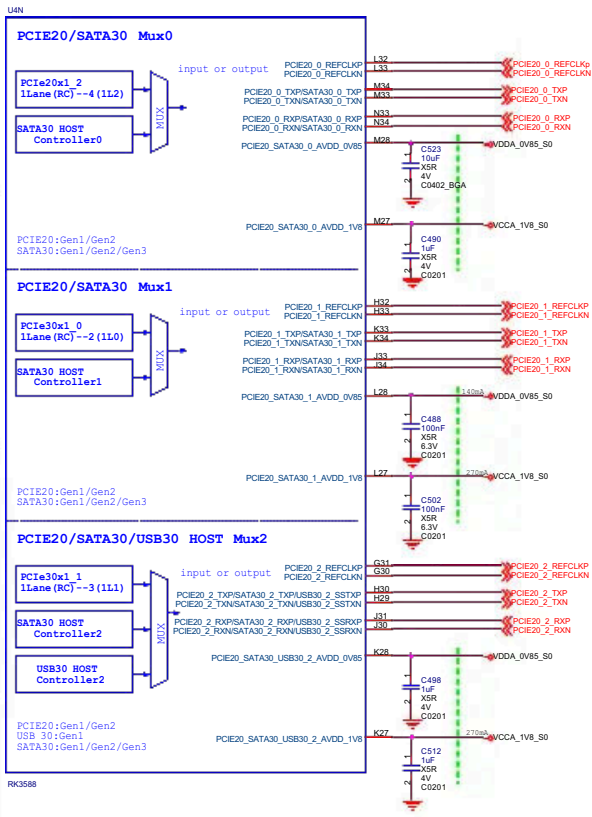


RK3588




RK3588

Shenzhen Xunlong Software Co., Ltd			
Project:	OP1 5 Ultra		
File:	17.RK3588_HDMIeDP Interface		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	8
		Of:	23



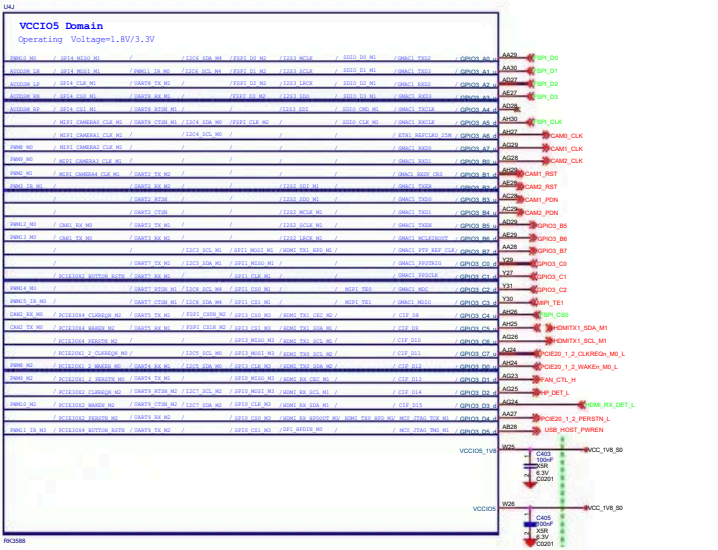
RK3588

RK3588

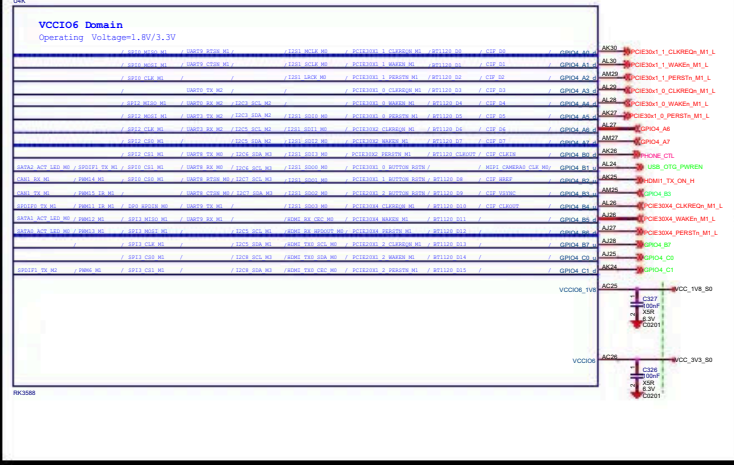


Shenzhen Xunlong Software Co., Ltd			
Project:	CPI 5 Ultra		
File:	18.RK3588_PCIE30PCIE20SATA30		
Date:	Monday, January 13, 2025	Rev:	V1.0
Sheet:	A3	Sheet:	9 of 28

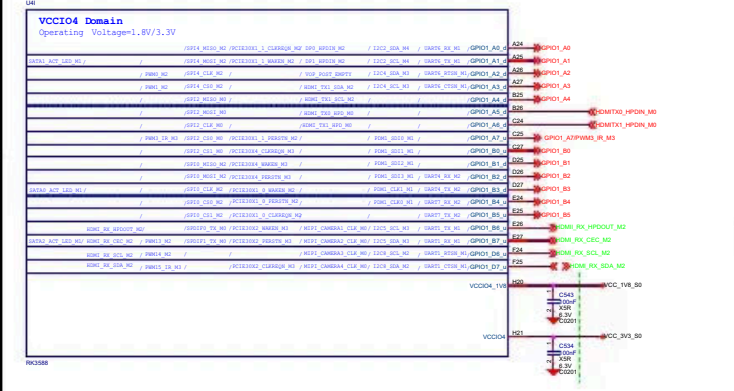
RK3588_J (VCCIO5 Domain)



RK3588_K (VCCIO6 Domain)

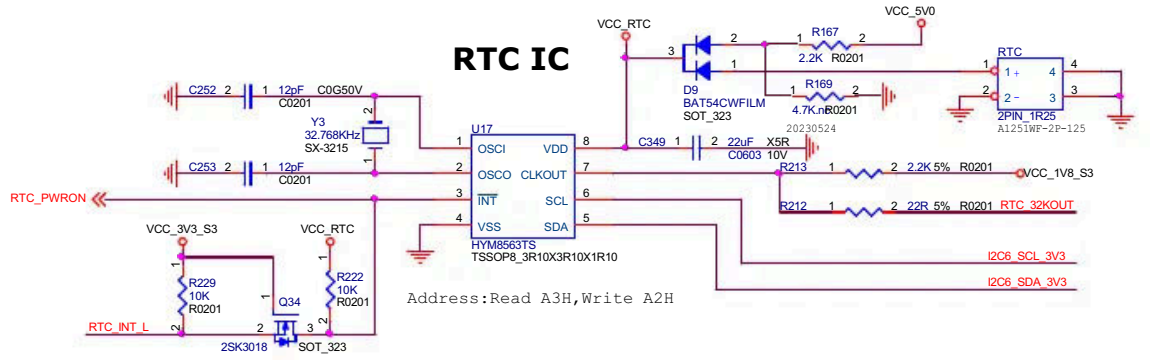


RK3588_I (VCCIO4 Domain)

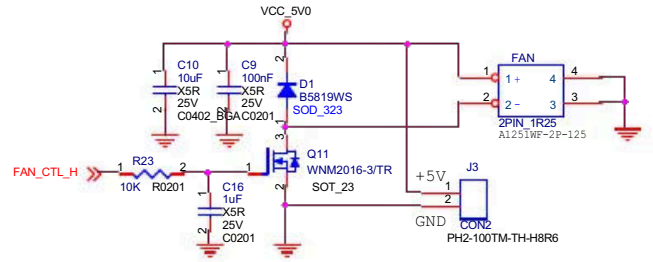


Shenzhen Xunlong Software Co., Ltd
 Project: OPIS Ultra
 File: RK3588_I_V1.0_V3.3V_GPI0
 Date: Monday, January 14, 2025 10:05:19 AM
 Size: A3 | Sheet: 16 | Cell: 28

I2C6_SDA_3V3
 I2C6_SCL_3V3
 RTC_INT_L
 RTC_32KOUT



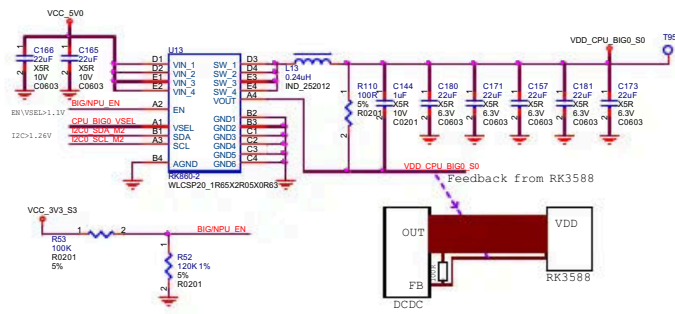
FAN_POWER



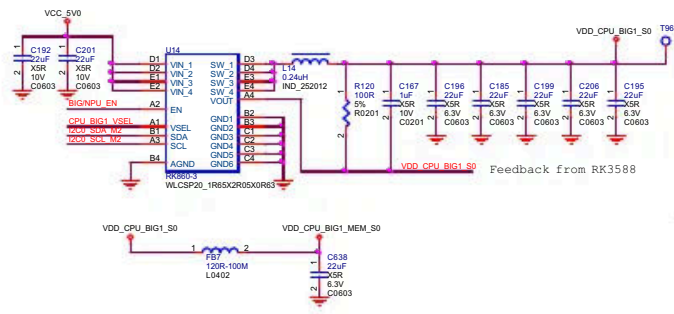
Shenzhen Xunlong Software Co., Ltd

Project:	OPI 5 Ultra		
File:	20.RTC/FAN		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	11
		Of:	28

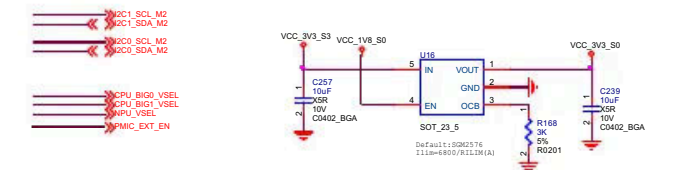
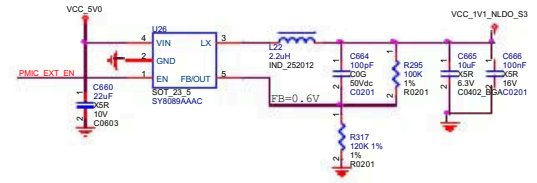
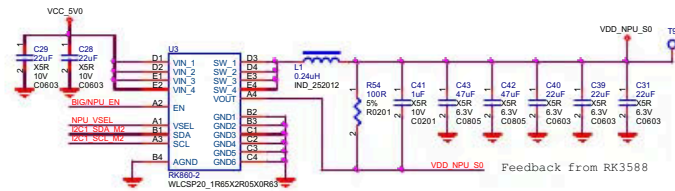
VDD_CPU_BIG0



VDD_CPU_BIG1



VDD_NPU

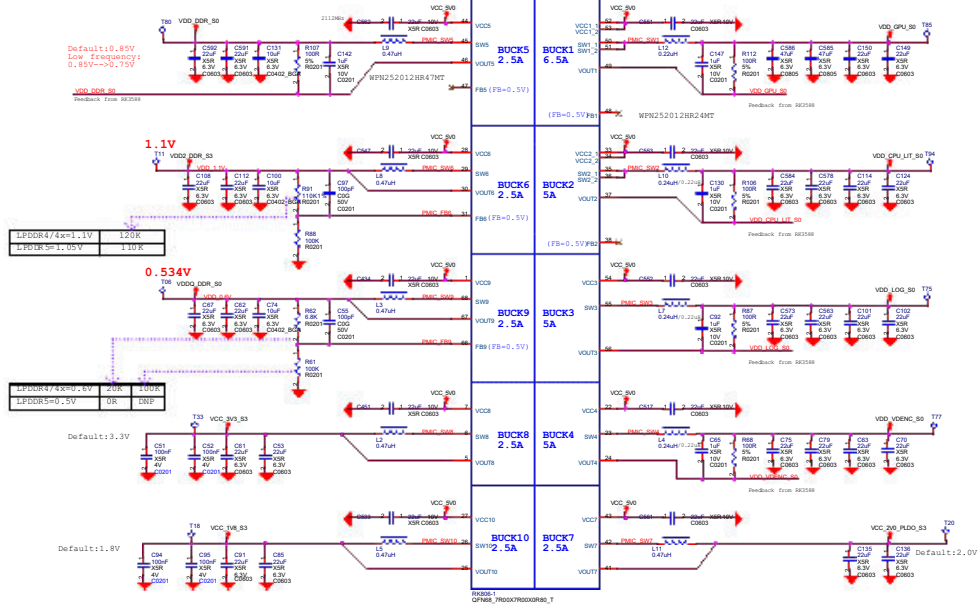


Shenzhen Xunlong Software Co., Ltd

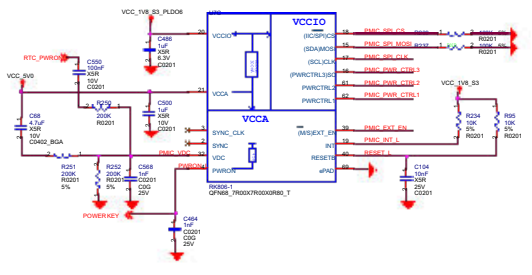
Project:	OP1 5 Ultra
File:	21Power_Est_Discrete
Date:	Monday, January 13, 2025
Rev:	V1.0
Size:	A3 Sheet: 12 Of: 23

PMIC RK806-1 BUCK

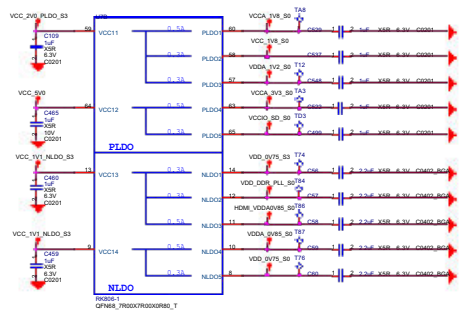
- PMIC_BK_CS
- PMIC_BK_VDSB
- PMIC_BK_CLK
- PMIC_PWR_CTRL1
- PMIC_PWR_CTRL2
- PMIC_PWR_CTRL3
- PMIC_INT_L
- PMIC_INT_H
- PMIC_EXT_BN



PMIC RK806-1 Management

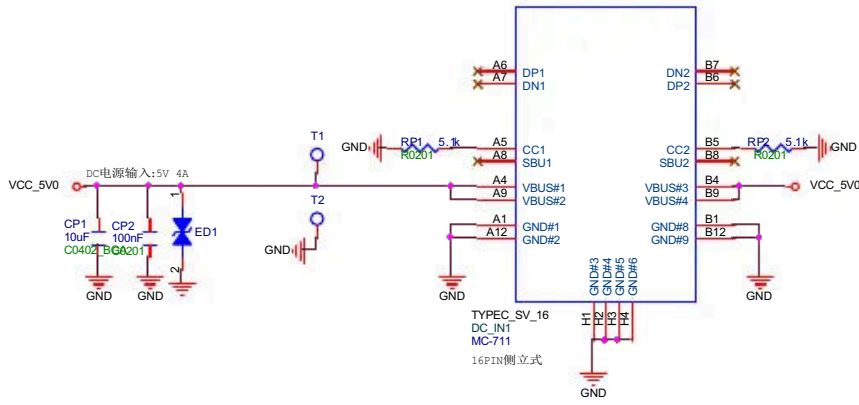


PMIC RK806-1 LDO



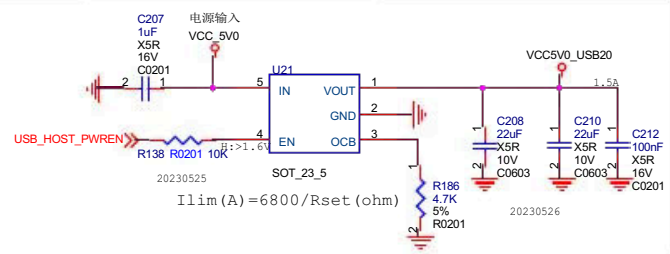
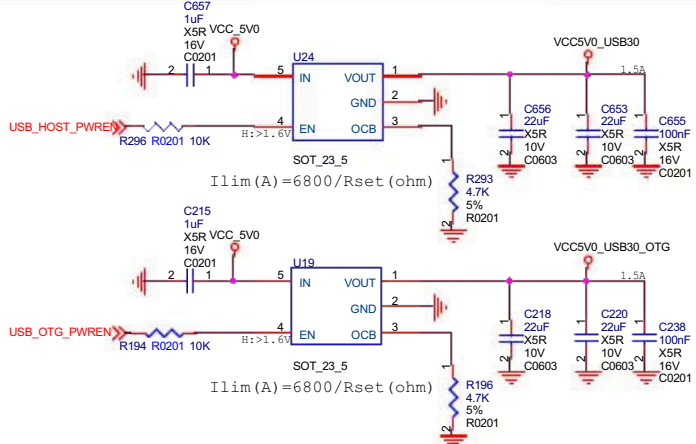
Shenzhen Xunlong Software Co., Ltd
 Product: Lipo 6 Ultra
 File: 22-Power-PMIC_RK806-1
 Date: Monday, January 15, 2024 10:51
 Drawn: xunlong

TPYE-C POWER IN

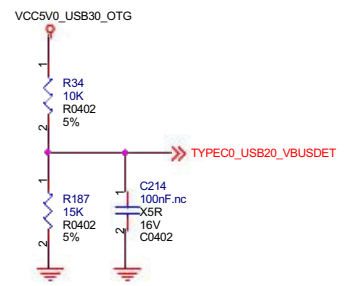
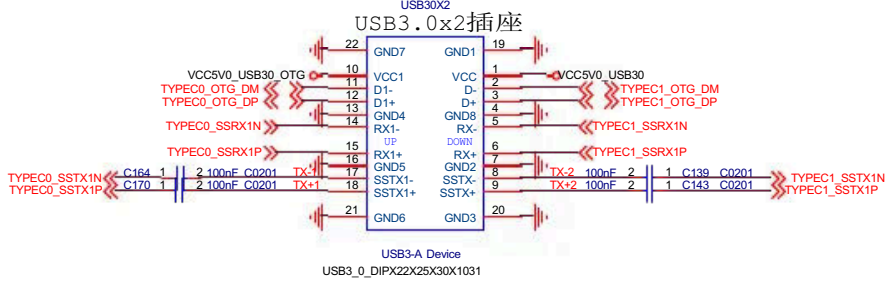


Shenzhen Xunlong Software Co., Ltd

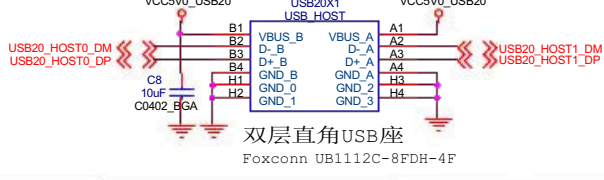
Project:	OPI 5 Ultra		
File:	23.Type C/DCIN		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	14 Of: 28



USB3.0*2



USB2.0*2

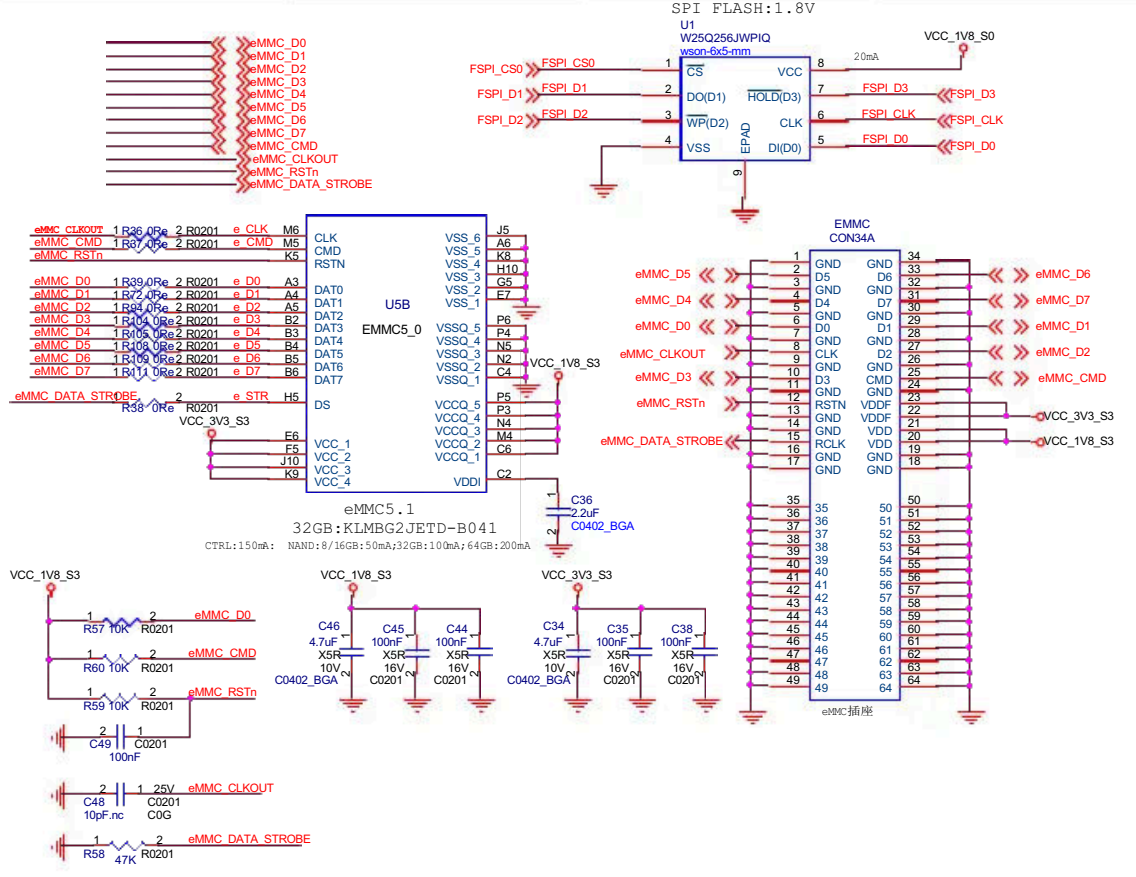


Shenzhen Xunlong Software Co., Ltd

Project:	OPI 5 Ultra		
File:	24.USB30/USB20		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	15
		Of:	28

eMMC Flash

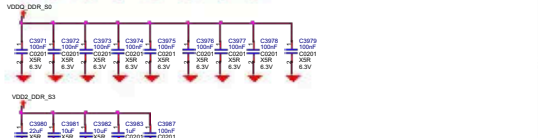
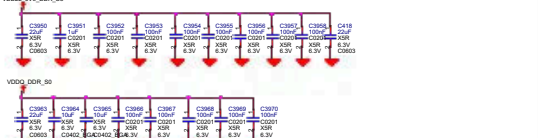
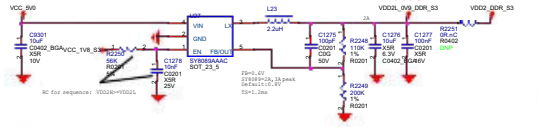
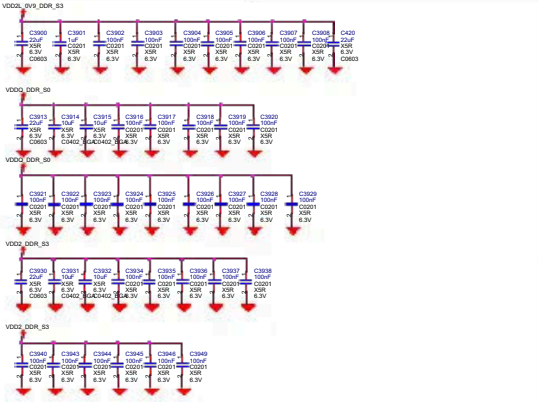
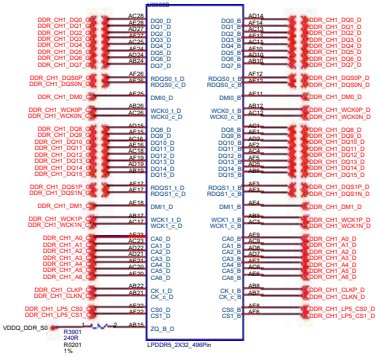
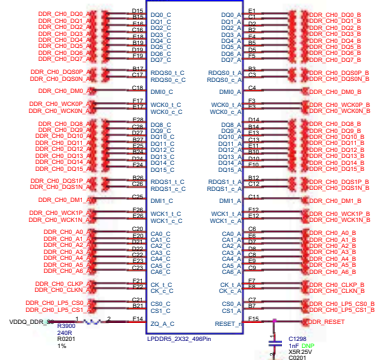
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A2	NC 2	P7
A8	NC 3	K10
A9	RFUNC_13	K7
A10	NC 4	K10
A11	NC 5	RFUNC_11
A12	NC 6	RFUNC_10
A13	NC 7	RFUNC_9
A14	NC 8	RFUNC_8
B1	NC 9	RFUNC_7
B7	NC 10	RFUNC_6
B8	NC 11	RFUNC_5
B9	NC 12	RFUNC_4
B10	NC 13	RFUNC_3
B11	NC 14	RFUNC_2
B12	NC 15	RFUNC_1
B13	NC 16	
B14	NC 17	
C1	NC 18	NC 107
C3	NC 19	NC 106
C5	NC 20	NC 105
C7	NC 21	NC 104
C8	NC 22	NC 103
C9	NC 23	NC 102
C10	NC 24	NC 101
C11	NC 25	NC 100
C12	NC 26	NC 99
C13	NC 27	NC 98
C14	NC 28	NC 97
D1	NC 29	NC 96
D2	NC 30	NC 95
D3	NC 31	NC 94
D4	NC 32	NC 93
D12	NC 33	NC 92
D13	NC 34	NC 91
D14	NC 35	NC 90
E1	NC 36	NC 89
E2	NC 37	NC 88
E3	NC 38	NC 87
E12	NC 39	NC 86
E13	NC 40	NC 85
E14	NC 41	NC 84
F1	NC 42	NC 83
F2	NC 43	NC 82
F3	NC 44	NC 81
F12	NC 45	NC 80
F13	NC 46	NC 79
F14	NC 47	NC 78
G1	NC 48	NC 77
G2	NC 49	NC 76
G12	NC 50	NC 75
G13	NC 51	NC 74
G14	NC 52	NC 73
H1	NC 53	NC 72
H2	NC 54	NC 71
H3	NC 55	NC 70
H12	NC 56	NC 69
H13	NC 57	NC 68
H14	NC 58	NC 67
J1	NC 59	NC 66
J2	NC 60	NC 65
J3	NC 61	NC 64
	NC 62	NC 63



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Project:	OPI 5 Ultra
File:	25_eMMC/SPI Flash
Date:	Monday, January 13, 2025
Rev:	V1.0
Size:	A3 Sheet: 16 Of: 28

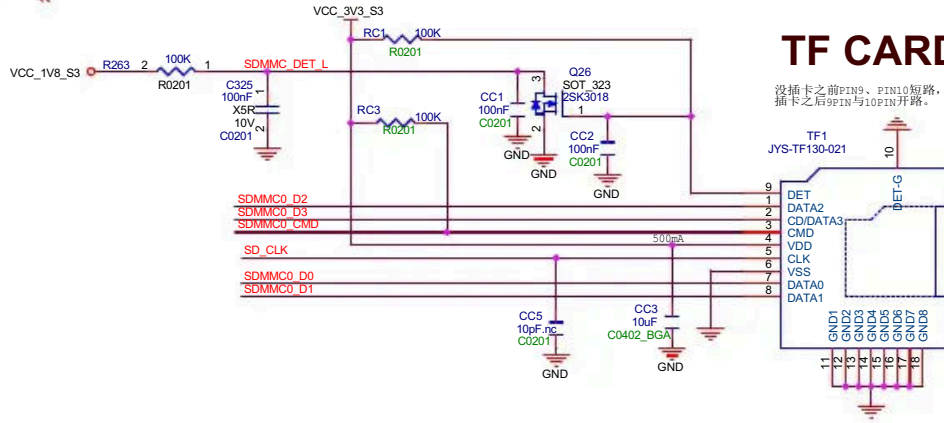
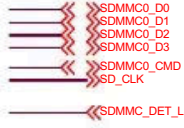
DRAM-LPDDR5X_2X32bit



Power sequence: VDD1>VDD2H>VDD2L>VDDQ=200mV

VDD1: 1.70V-1.95V
 VDD2H: 1.81V-1.12V
 VDD2L: 0.87V-0.97V
 VDDQ: 0.47V-0.57V

TF CARD



TF CARD

没插卡之前PIN9、PIN10短路。
插卡之后9PIN与10PIN开路。

Rockchip Confidential



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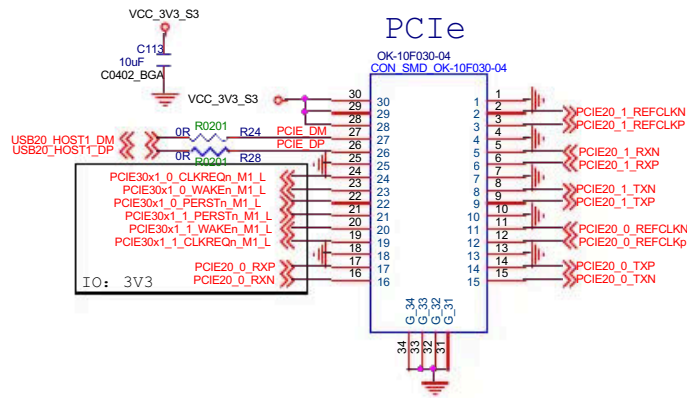

Project:	OPI 5 Ultra		
File:	27.Flash-TF Card		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	18 Of: 28

D

C

B

A

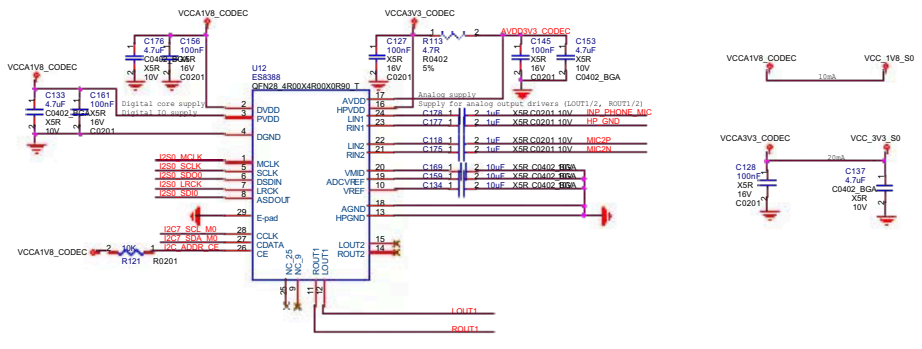



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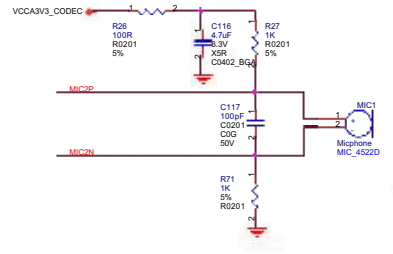
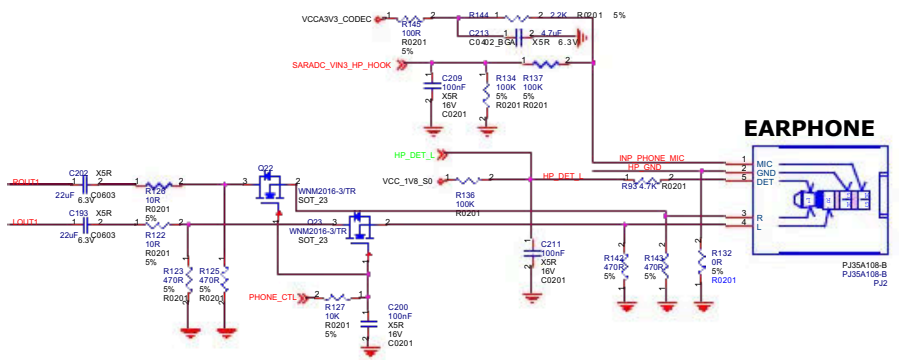
Project:	OPI 5 Ultra		
File:	28..EXT_30PIN_PCIe		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	19 of 28

CODEC ES8388

- ⚡ I2C7_SDA_M0
- ⚡ I2C7_SCL_M0
- ⚡ I2S0_MCLK
- ⚡ I2S0_SCLK
- ⚡ I2S0_LRCK
- ⚡ I2S0_SDD0
- ⚡ I2S0_SDD1

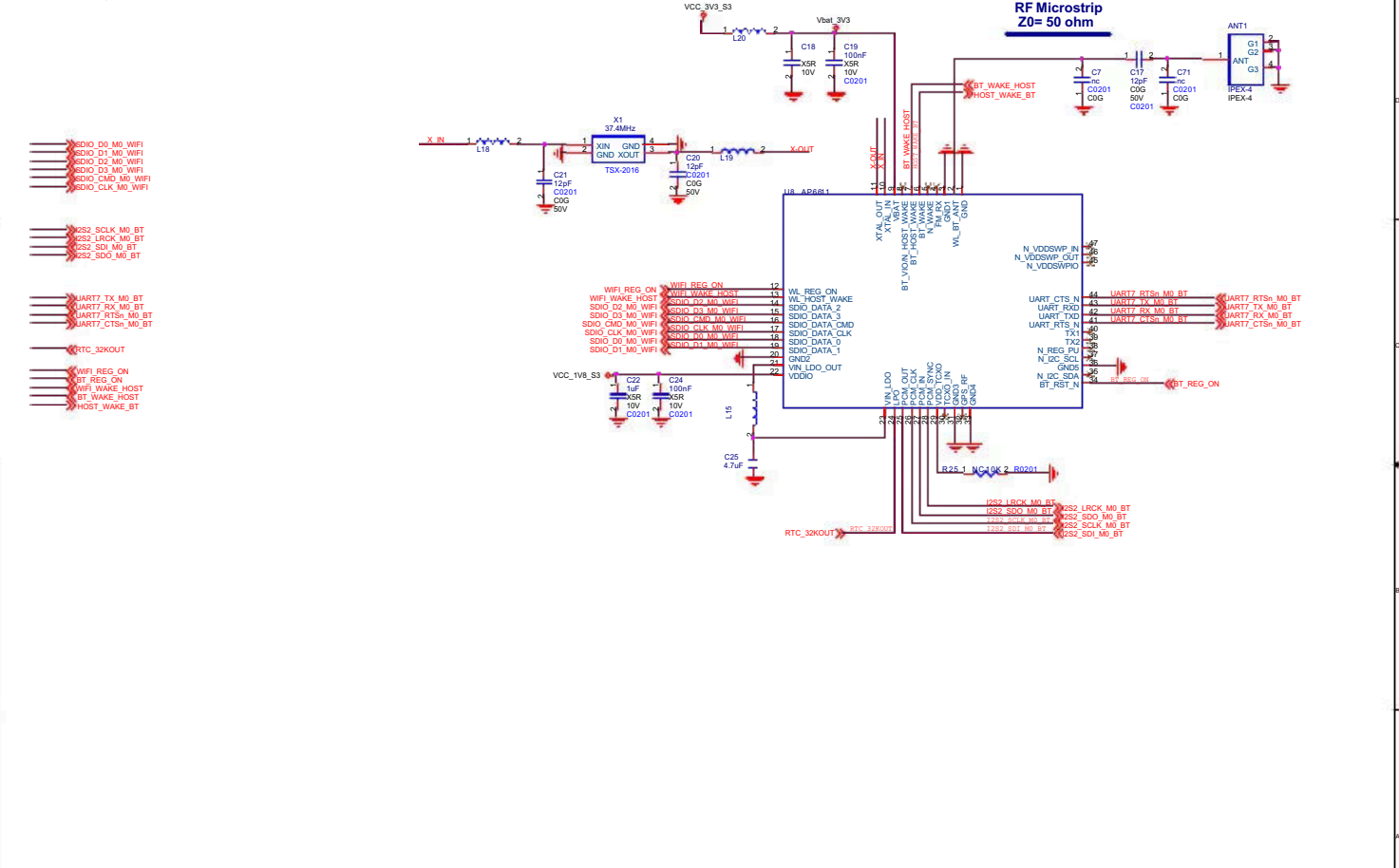


EARPHONE

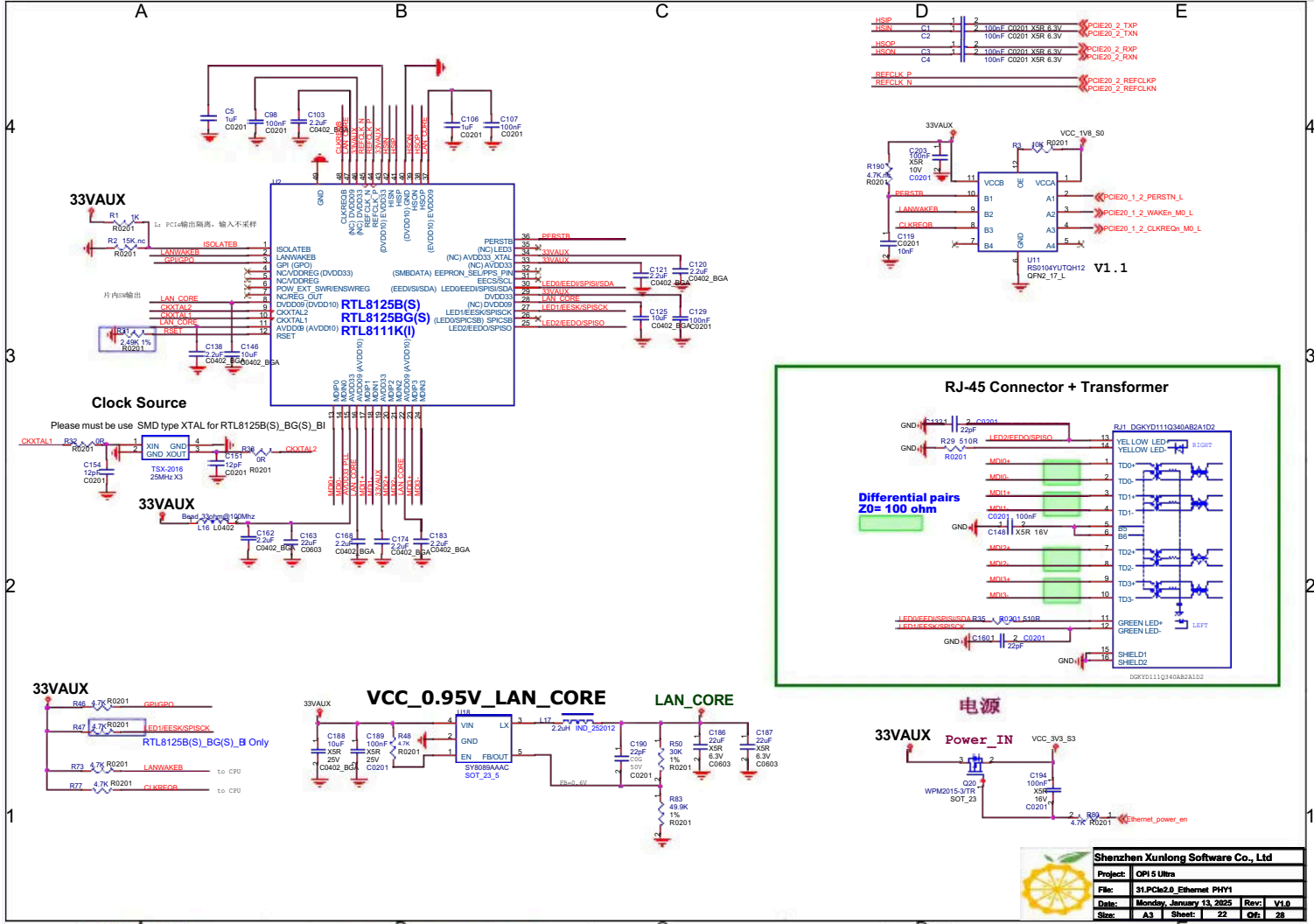


Shenzhen Xunlong Software Co., Ltd			
Project:	OPI 6 Ultra		
File:	28.Audio Codec		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	20
		Of:	28

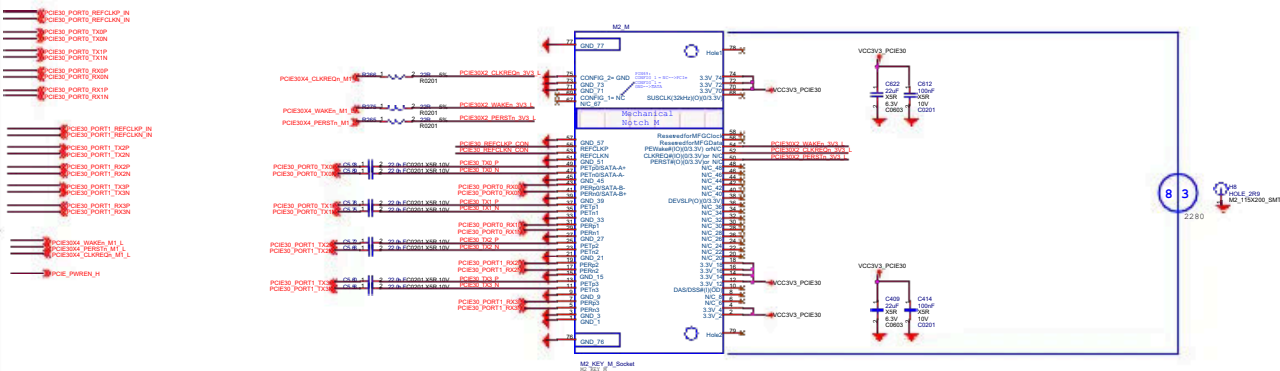
SDIO WIFI/BT Module-1T1R



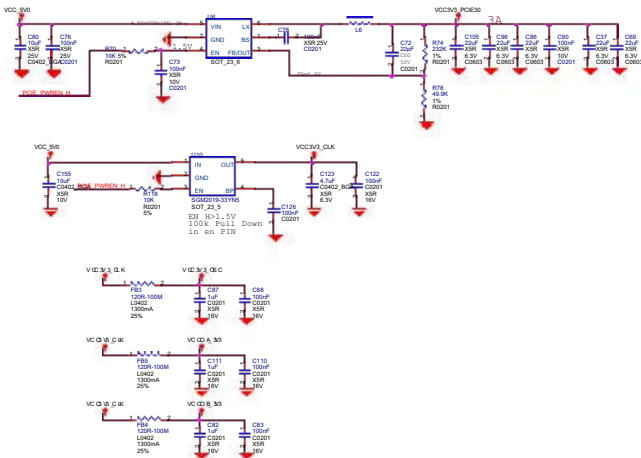
Shenzhen Xunlong Software Co., Ltd			
Project:	OPI 5 Ultra		
File:	36.WIFI/BT-SDIO_1T1R-HART		
Date:	Monday, January 13, 2025	Rev:	V1.0
Size:	A3	Sheet:	21 of 28



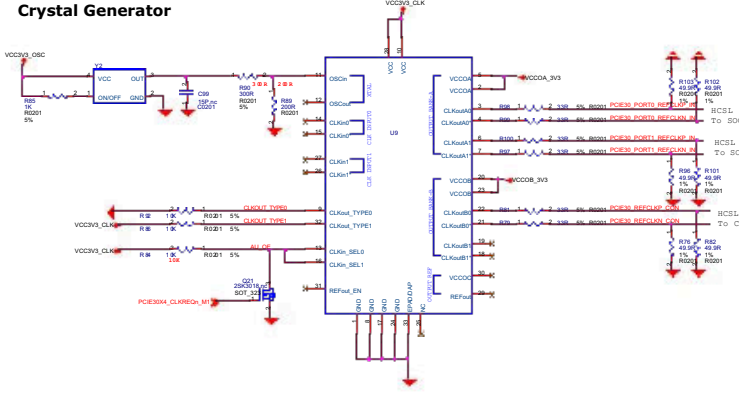
M.2 PCIe3.0 x 2Lanes



M.2 Power



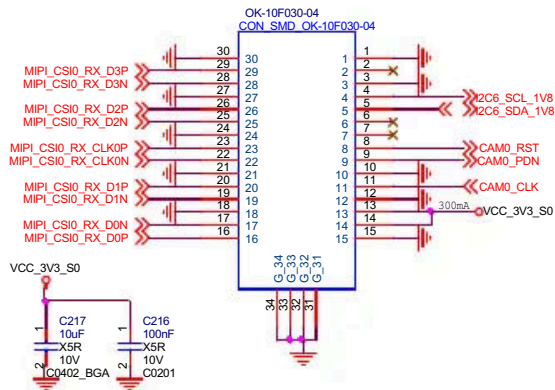
Crystal Generator



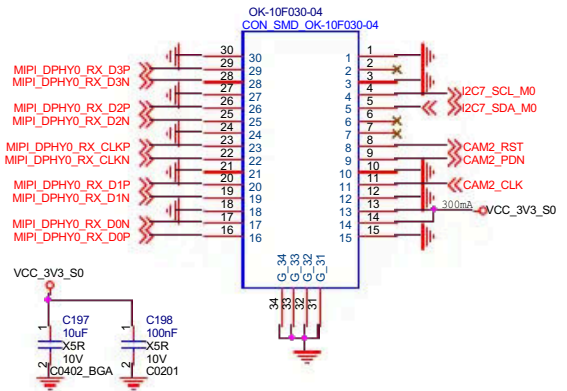
Shenzhen Xianglong Software Co., Ltd
 Project: XPL6Ultra
 File: SPCIM42_IMEY_PCB.LPC
 Date: Monday, January 15, 2024 10:28:29
 Layer: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32

MIPI-CSIO_RX

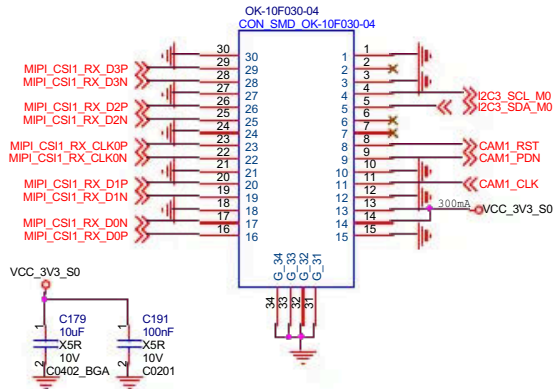
CAM0



CAM2



CAM1

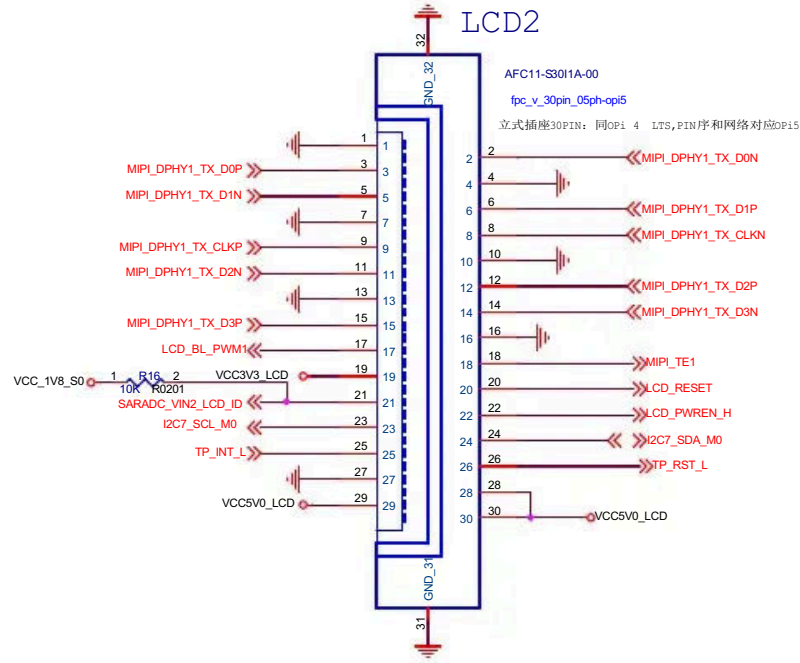


Shenzhen Xunlong Software Co., Ltd

Project: OPI 5 Ultra			
File: 33.VI-Camera_MIPI_CSI-RX			
Date: Monday, January 13, 2025	Rev: V1.0		
Size: A3	Sheet: 24	Of: 28	

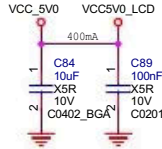
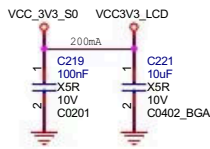
MIPI DPHY1 TX

LCD2



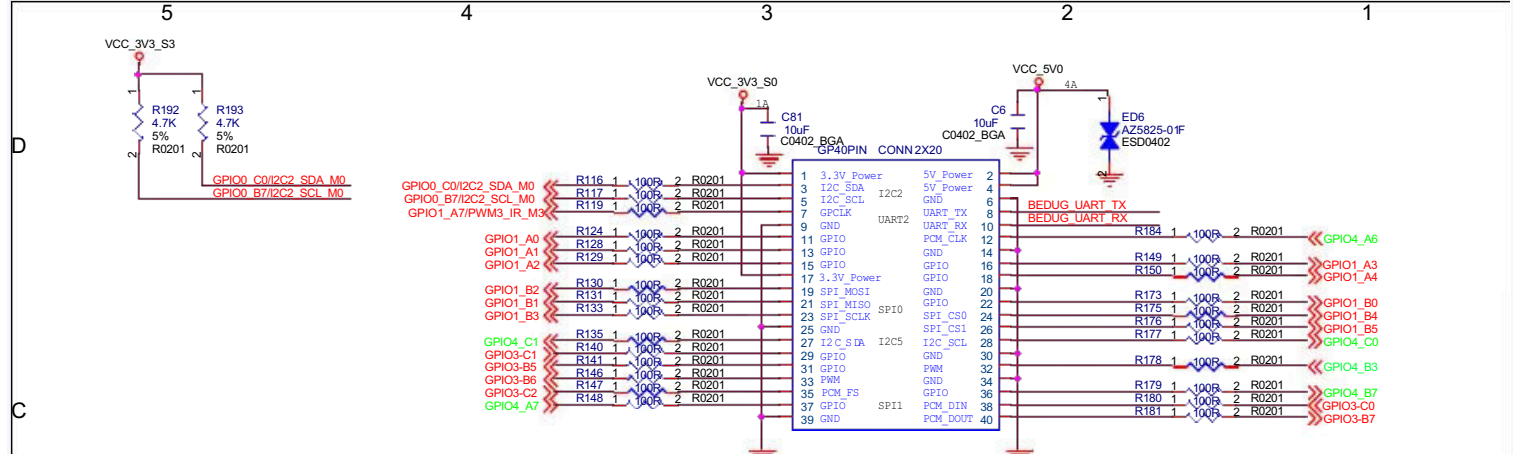
FFC Pin List

- Pin1 : GND
- Pin2 : DON
- Pin3 : D0P
- Pin4 : GND
- Pin5 : D1N
- Pin6 : D1P
- Pin7 : GND
- Pin8 : CLKN/AUXN
- Pin9 : CLKP/AUXP
- Pin10 : GND
- Pin11 : D2N
- Pin12 : D2P
- Pin13 : GND
- Pin14 : D3N
- Pin15 : D3P
- Pin16 : GND
- Pin17 : LCD_PWM_BL
- Pin18 : LCD_TE
- Pin19 : VCC3V3_LCD
- Pin20 : LCD_RST
- Pin21 : LCD_ID
- Pin22 : LCD_PWREN
- Pin23 : TP_I2C_SCL
- Pin24 : TP_I2C_SDA
- Pin25 : TP_INT
- Pin26 : TP_RST
- Pin27 : GND
- Pin28 : 5V0
- Pin29 : 5V0
- Pin30 : 5V0

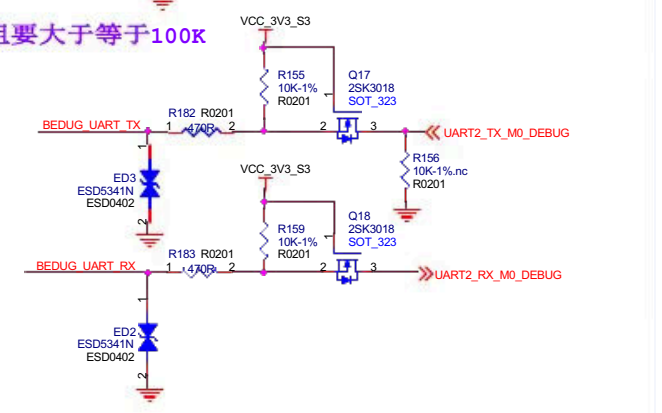
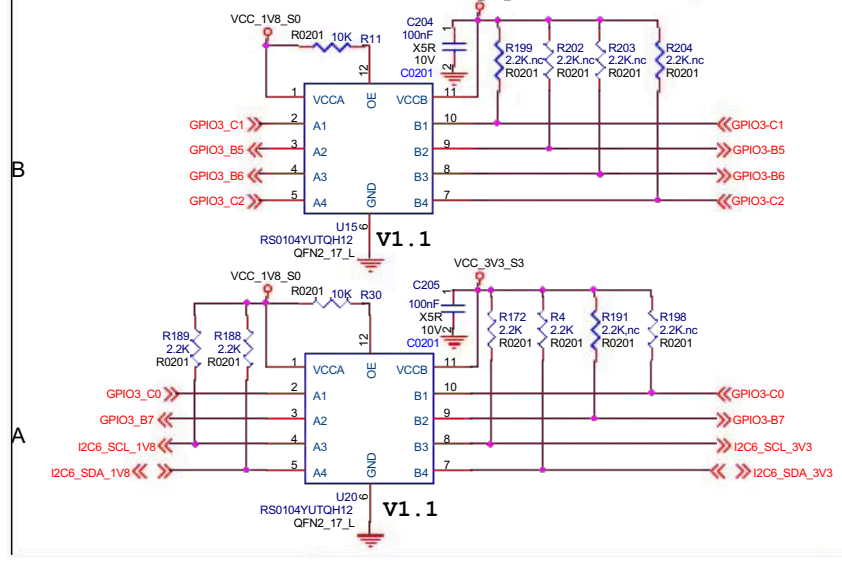


Shenzhen Xunlong Software Co., Ltd

Project:	OPI 5 Ultra		
File:	35.VO-LCM_MIPI		
Date:	Monday, January 13, 2025	Rev:	V1.0
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注：外部上下拉电阻要大于等于100K



Shenzhen Xunlong Software Co., Ltd

Project: OPI 5 Ultra

File: 36.EXT_GPIO40/DEBUG

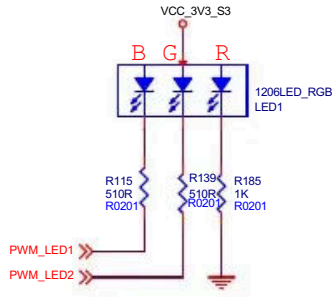
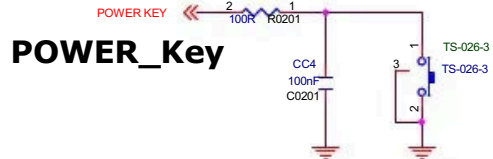
Date: Monday, January 13, 2025 Rev: V1.0

Size: A3 Sheet: 27 Of: 28

BOOT



POWER1



				Shenzhen Xunlong Software Co., Ltd			
				Project: OPI 5 Ultra			
File: 37 KEY/LED				Date: Monday, January 13, 2025		Rev: V1.0	
Size: A3		Sheet: 28		Of: 28			